MULTIPLE-GATE DEVICE WITH FLOATING BACK GATE

Abstract

Disclosed is a multiple-gate transistor that includes a channel region and source and drain regions at ends of the channel region. A gate oxide is positioned between a logic gate and the channel region and a first insulator is formed between a floating gate and the channel region. The first insulator is thicker than the gate oxide. The floating gate is electrically insulated from other structures. Also, a second insulator is positioned between a programming gate and the floating gate. Voltage in the logic gate causes the transistor to switch on and off, while stored charge in the floating gate adjusts the threshold voltage of the transistor. The transistor can comprise a fin-type field effect transistor (FinFET), where the channel region comprises the middle portion of a fin structure and the source and drain regions comprise end portions of the fin structure.